AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An ~~improved~~ interface system for synchronous hierarchy telecommunication networks comprising a high frequency backpanel function, said system comprising:

at least a central board ~~(CM, CB1, CB2)~~ having an active or inactive state; and

one or more input/output peripheral boards ~~(PD)~~ for exchanging data frames ~~(TRM1, TRM2, TRU1, TRU2)~~ and control bytes over a connection between a peripheral board and a central board ~~,(A1, A2, SY, H4, L),~~

wherein said data frames ~~(TRM1, TRM2, TRU1, TRU2)~~ contain said control bytes, ~~(A1, A2, SY, H4, L);~~ comprising at least one of bytes indicating frame alignment, bytes indicating synchronization, and bytes monitoring the connection and switching of the state of said central board, and wherein said data frames ~~(TRM1, TRM2, TRU1, TRU2)~~ are bitwise converted before being exchanged between the peripheral boards ~~(PD)~~ and the central board ~~(CM, CB1, CB2)~~.

2. (currently amended): An interface system according to claim 1, wherein the central board ~~(CM, CB1, CB2)~~ comprises a local clock ~~(OL1, OL2)~~.

3. (currently amended): An interface system according to claim 2, wherein said control bytes ~~(A1, A2, SY, H4, L)~~ comprise the bytes ~~for~~ indicating frame alignment ~~(A1, A2)~~.

4. (currently amended): An interface system according to claim 2, wherein said control bytes ~~(A1, A2, SY, H4, L)~~ comprise the ~~synchronism~~ bytes indicating synchronization~~(SY, H4)~~.

5. (currently amended): An interface system according to claim 2, wherein said control bytes ~~(A1, A2, SY, H4, L)~~ comprise the bytes ~~for~~ monitoring the connection and switching of the active board ~~(L)~~.

6. (currently amended): An interface system according to claim 1, wherein it provides further signalling bytes ~~(TP, HP, LP)~~ inserted in the various layers of said data frames ~~(TRM1, TRM2)~~ for implementing a mapping function of said ~~the~~ data frames ~~(TRM1, TRM2)~~ and in-band signalling.

7. (currently amended): An interface system according to claim 1, wherein a ~~the~~ switch matrix ~~(CM)~~ comprises at least two central boards ~~(CB1, CB2)~~, whose local clocks ~~(OL1, OL2)~~ are made interdependent through ~~the~~ exchange of time information ~~(IT)~~.

8. (currently amended): An interface system according to claim 7, wherein said time information ~~(IT)~~ contains the frequency of clock signals ~~(CKR1 ,CKR2)~~ of the local clocks ~~(OL1, OL2), information about frame alignment (SY),~~ and information of said synchronization~~about multiframe synchronism (H4)~~.

9. (currently amended): An interface system according to claim 7, wherein the peripheral boards ~~(PD)~~ comprise memory means ~~(MSA, OCNT)~~ for compensating jitter or wander effects on the frame alignment.

10. (currently amended): An interface system according to claim ~~7~~ 9, wherein said memory means ~~(MS; OCNT)~~ and said time information ~~(IT)~~ cooperate for implementing a hitless traffic protection.